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Reducing Switch Count in a Self-Balancing Nine-Level Switched Capacitor Inverter: A Modified Approach

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ABSTRACT

Renewable energy sources are becoming more and more popular to minimize environmental damage while meeting the world's expanding demand for electricity. However, components like DC-AC converters, trans- former/inductor absence operation, front-end DC-DC converters with high gain capacity, and high voltage at a selected level are needed for small-scale PV solar independent AC loads and for grid applications as well as. This study offers a step-up boost inverter with quadruple operation of 9-levels that solves the problem by using a switched capacitor approach with less complications. By utilizing the control scheme itself, the topology is intended to balance capacitor voltages without the requirement for sensors. A phase disposition- pulse width modulation (PD-PWM) control technique is employed in this topology. This work focuses on the switching operation modes of the anticipated inverter and presents experimentally confirmed simulation experiments carried out in MATLAB/Simulink. All things considered; this research presents a viable option for renewable energy systems that can assist in satisfying the demand for electricity while preserving the environment.

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1. INTRODUCTION

The global electricity demand is increasing rapidly, but the predominant means of electrical energy generation, such as the combustion of fossil fuels and nuclear materials, result in the emission of harmful gases that contribute to environmental imbalances on a global scale. To address this challenge, there is a growing interest in adopting renewable energy sources that are environmentally friendly. However, renewable energy generation stations are often situated at a considerable distance from load centers, resulting in amplified transmission and distribution losses during the delivery of electrical energy [1]-[3]. Rooftop distributed solar photovoltaic (PV) systems have been presented recently as a solution to this problem. These systems typically exhibit power and voltage ratings in the

range of 0.5 kW to 5 kW and 60-100 V, respectively. Rooftop PV systems are becoming increasingly popular, and the number of units is expected to reach 100 million by 2030, which could be achieved by maintaining today's yearly installation rate. Rooftop PV systems offer numerous benefits, including reduced transmission and distribution losses, lower capital and operational costs, and lower maintenance requirements. The paper suggests a modified nine-level inverter that achieves all of the aforementioned objectives with fewer components by using a switched capacitor approach. The topology is designed to balance capacitor voltages without the need for sensors, using the control scheme itself. A Phase disposition Pulse Width Modulation (PDPWM) is handled as the control scheme for the proposed topology. Overall, rooftop PV systems offer a promising solution for renewable energy systems that can help meet electricity demands while maintaining a clean and green environment [4].

The increasing demand for electrical energy is met by conventional energy sources, which harm the environment. To address this issue, renewable energy sources are becoming more popular. Installing distributed solar photovoltaic (PV) systems on rooftops has been a novel way to lower transmission and distribution losses when the power is transferring from various generation stations to local load centers [5]-[8]. In a step-up 9-level inverter employing a technique of switched capacitor (SC) and requires fewer components is proposed to address the challenges of rooftop PV systems. The topology is designed to balance capacitor voltages without the need for sensors, using the control scheme itself. The multilevel inverter (MLI) is a power conversion technology used in power electronics and renewable energy systems. The necessity of DC-AC conversion and high-gain DC-DC converters to match AC grid voltage levels is covered in the article. The various types, such as MLI's of diode-clamped, flying-capacitor [9]-[11], and cascaded H-bridge (CHB) [12]-[14] are also discussed along with the modifications made to lessen the reliance on isolated DC sources, address capacitor voltage balancing issues, and minimize the number of switches [15]-[18]. It is reported that the SC enabled MLIs are well-suited for RE system applications, including small scale solar PV rooftops [19].

A boost- SC inverter by arranging in a Marx structure manner that employs SC techniques to increase the number of output voltage levels [14]. The Marx structure units enhance the output voltage levels when added to the H-bridge. Other advancements in MLIs have been proposed in [16] to overcome challenges such as capacitor unbalancing, reduced switch count, and improved voltage levels. For example, a cascaded MLI using separate DC voltage sources for the front-end and back-end units has been proposed in [16]. Switched capacitor techniques are used by the front-end unit, while an H-bridge unit is used by the lateral end. The number of layers is increased by cascading these units together. Furthermore, a hybrid SC-MLI [17] consists of one capacitor, two complementary switches placed in parallel or series, and single DC voltage gives a greater number of levels of voltages.

Multilevel inverters (MLIs) frequently employ switched capacitor techniques to provide the desired output voltage levels. Several methods for designing MLIs with switched capacitor techniques have been put forth. To explain this, let us consider a voltage boost MLI of general purpose, which consists of number of series and parallel switches to the input and output points along diodes and capacitors [18]. As in the ref [19], one should note that the intended output voltage levels can be produced by an inductor incorporated into the resonance circuit of a quasi-resonant MLI. An arrangement of repeated switching capacitor units of cross-connection at the end of two T-type circuits is useful to find out the output voltage levels [19]-[23]. The work presented in [22] pacts a DC-source cascaded H- bridge MLI. Using switched capacitor techniques, output voltage levels are achieved by substituting isolated DC voltage sources with capacitors. Series/parallel conversion inverter for a hybrid nine-level inverter is introduced [23]. This inverter can increase voltage levels while passively balancing capacitor voltage to maintain a steady voltage. In [24], a generalized inverter topology with an active neutral point clamped (ANPC) gain1 is shown. By adding switches and capacitors, various voltage levels can be enabled. The authors of the work [23]-[26] are presented with a generic five-level inverter to increase the number of output voltage levels as compared to the earlier level inverters and which consists of four switches and a capacitor module.

Several novel multilevel inverter (MLI) topologies have been put forth in an effort to solve the problems that arise in applications involving renewable energy. The ref [25] demonstrates a hybrid T-type nine-level inverter with triple gain, in which it uses special arrangements of switches, diodes, and capacitors to provide the required voltage levels. Another invention that was introduced in [26] is the

generalized CGSC- TL architecture, which provides various configurations of switches, diodes, and capacitors to generate the required volt- age levels. By modifying the boost converter as an MLI using series/parallel combinations of switches, diodes, and capacitors, the CGT9L boost inverter—which was first announced in [27]—provides common grounding between the DC source and the output AC. Furthermore, the method discussed in the ref [28] creates output levels by fusing two units: an H-bridge unit and a generating unit with circuit components. A 7-level SC (7-LSC) architecture with gain-3 was introduced in [29], a MLI topology with switches of unipolar in bi-directional and bipolar in unidirectional direction was offered in [30]. Because the capacitors are naturally capable of self-balancing voltage, these topologies do not command sensor units to sense and assess the voltage between different capacitors [30]-[34]. This research concludes with the introduction of a new topology that has fewer components than current competitor topologies. The following points indicate the contributions of the manuscript:

- A 9-level SC based MLS topology is advised with a fewer number of switches and capacitors and simulated the same by utilizing MATLAB.
- A self-balancing scheme for capacitors is introduced with a phase disposition PWM control strategy.

2. PROPOSED INVERTER TOPOLOGY

As shown in Figure 1, the inverter consists of mainly a source of DC voltage, capacitor numbers- two (C1, C2), and electronic switches of eight. One of the switches operates bidirectionally (S6), while the remaining seven switches function unidirectionally (S1to S8).

The switches S7, S8, S1, and S2 work together to prevent short-circuit damage between the source and capacitors. The C1 and C2 are charging and discharging in parallel and series with the DC voltage source ensures the desired output voltages. Particularly, self-balanced voltages across capacitors C1 and C2 are produced by charging and discharging them to +1Vdc and +2Vdc, respectively. Across the load, the output voltage levels can be ± 1 to ±4 Vdc. Capacitors are charged and discharged using the earlier stated techniques of parallel/series, which guarantee capacitors in balanced mode and achieve the desired voltage levels using a single DC source via a precise switching pattern. To generate all voltage levels except zero, a total of six switches are continually toggled ON in conjunction with the discharged capacitor. To reach zero, turn on the 2 switches on the upper/positive sign arm or the lower/negative sign arm.

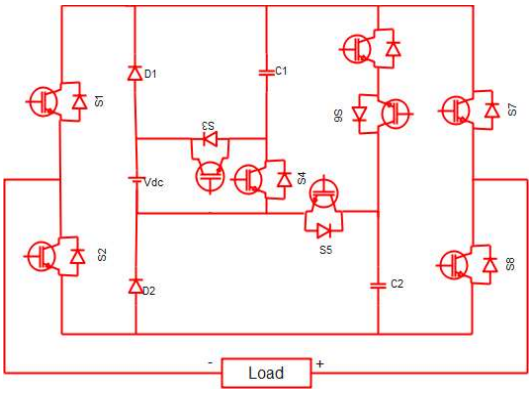


Figure 1. Architecture of proposed 9-level MLI.

2.1 Operating modes:

A. Zero Voltage Levels:

In this work, two approaches for reaching the zero-voltage level with the suggested topology: either by turn-on the lower arm switches (S8, S2) or by the upper arm switches (S7, S1). The creation of the 0 V level utilizing the upper side arm switches is shown in Figure 2(a).

B. Positive Voltage Levels:

To achieve the different voltage levels in the proposed topology, specific switches are activated in a particular sequence. The following describes the activation of switches to generate each voltage level:

Voltage Level of +1Vdc: The switches, S7 and S2 are activated to establish a series connection between the DC voltage source and the load. Simultaneously, switch S4 is engaged to facilitate the charging of capacitor C1 to +1Vdc. The C2 is left in a floating state (-), refraining from both charging and discharging. This arrangement ensures the transmission of +1Vdc to the load, as depicted in Fig 2(b).

Voltage Level of +2Vdc: The switches, S3, S7, and S2 are employed to create a series alignment among the DC voltage, capacitor C1, and the load. Additionally, switch S3 is activated to discharge capacitor C1 to +1Vdc, while switch S6 is turned on to charge capacitor C2 to +2Vdc. The outcome is the transmission of +2Vdc to the load, as illustrated in Fig 2(c).

Voltage Level of +3Vdc: The switches S2, S7, and S5 are activated to establish a series connection between DC voltage, capacitor C2, and the load. Concurrently, switch S5 is turned on to discharge capacitor C2 to +2Vdc. Meanwhile, capacitor C1 remains in a floating state (-), without undergoing charging or discharging. This configuration enables the transmission of +3Vdc to the load, as shown in Fig 2(d).

Voltage Level of +4Vdc: The S3, S7, S2, and S5 are activated to establish a series connection among the DC voltage, capacitor C1, capacitor C2, and the load. Switch S3 is then turned on to discharge capacitor C1 to +1Vdc, while switch S4 is activated to discharge capacitor C2 to +2Vdc. In this scenario, both capacitors release their stored energy, resulting in the transmission of +4Vdc to the load, as depicted in Fig 2(e).

C. Negative Voltage Levels:

To achieve negative voltage levels in the proposed topology, specific switches are activated in a particular sequence. The following describes the activation of switches to generate each negative voltage level: -1Vdc Voltage Level: Switches S1, S8, and S2 are activated to establish a series connection between the DC voltage source and the load. Additionally, switch S4 is engaged to charge capacitor C1 to +1Vdc, while capacitor C2 is maintained in a floating state (-), devoid of charging or discharging. This configuration facilitates the transmission of -1Vdc to the load, as depicted in Fig 2(f).

Voltage Level of -2Vdc: Switches S3, S8, and S2 are turned on to create a series arrangement involving the DC voltage source, capacitor C1, and the load. Furthermore, switch S3 is activated to discharge capacitor C1 to +1Vdc, and switch S6 is turned on to charge capacitor C2 to +2Vdc. This results in the transmission of - 2Vdc to the load, as illustrated in Fig 2(g).

Voltage Level of -3Vdc: Activation of switches S1, S8, and S5 establishes a series connection among the DC voltage source, capacitor C2, and the load. Simultaneously, switch S5 is turned on to discharge capacitor C2 to +2Vdc, while capacitor C1 is kept in a floating state (-) without undergoing charging or discharging. This arrangement enables the transmission of -3Vdc to the load, as shown in Figure 2(h).

Voltage Level of -4Vdc: The S3, S8, and S5 are activated to establish a series connection involving the DC voltage source, capacitor C1, capacitor C2, and eight triangular carriers and the load. Additionally, switch S3 is turned on to discharge the C1 to +1Vdc, and switch S4 is activated to discharge capacitor C2 to +2Vdc. In this scenario, these two capacitors to deliver their earlier stored energy, resulting in the transmission of -4Vdc to the load, as indicated in Figure 2(i).

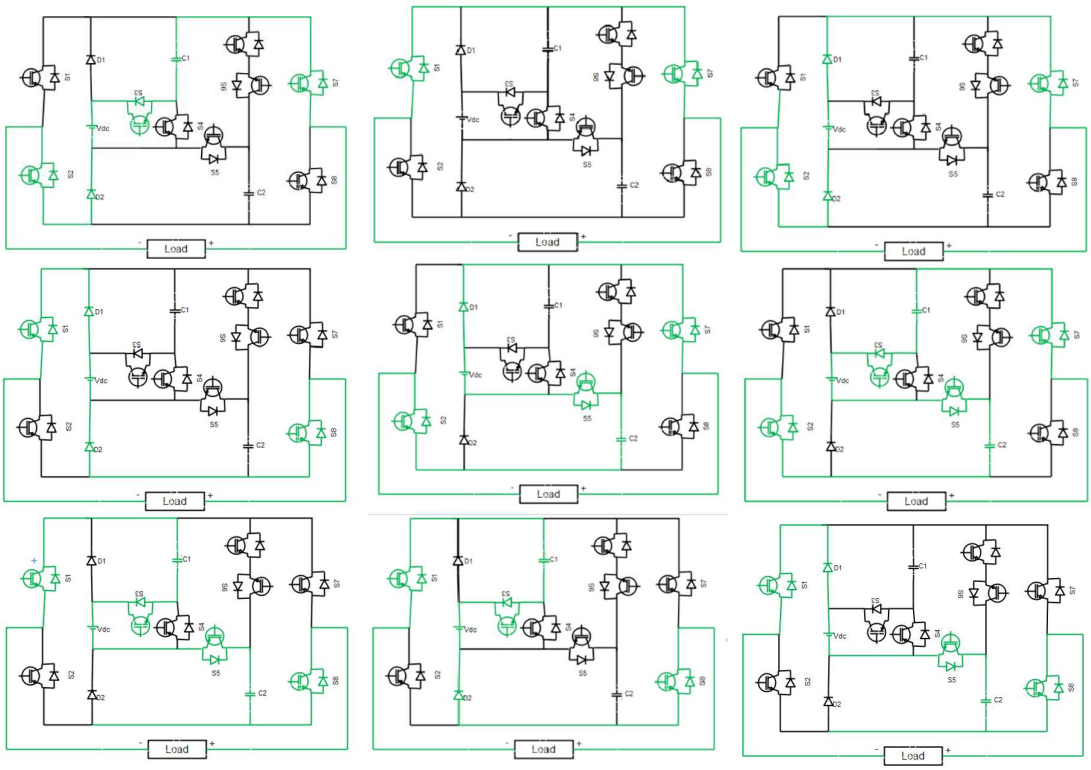


Figure 2. Operating modes of the 9-level MLI.

3. METHODOLOGY

The implementation utilizes level shifted- PWM (LS- PWM) to generate switching pulses. In this technique, the number of required carrier signals equal to the number of required level of output voltage minus one. The schema of level-shifted PWM is shown in Figure 3.

The LS-PWM employs a single sinusoidal modulating signal (M = Vmsin (2πfmt)) signals (Cr1 − Cr8). The com- parison between the modulating signal and carrier signals generates eight pulses (X1 − X8). During positive cycles, X1 compares M with Cr1, followed by X2 comparing M with Cr2, and so forth. Conversely, during negative cycles, X8 represents the comparison with Cr8, while X7 compares with Cr7, and so on. A switching table, as outlined in Table 1, establishes the logic pattern to generate appropriate switching pulses for the switches. One should note that the value of carrier signal amplitude remains constant, while the modulation signal amplitude adjusting from 0 to 4, facilitating the generation of various modulation index values (Ma = 0.4, 0.7, and 0.9).

Table 1. ON and OFF Stages of Switching stages.

Switches (S1 to S8)									
	+4Vdc	**+3Vdc**	**+2Vdc**	**+Vdc**	**0 Vdc**	**-Vdc**	**-2Vdc**	**-3Vdc**	**-4Vdc**
1	0	0	0	0	1	1	1	1	1
2	1	1	1	1	0	0	0	0	0
3	1	0	1	0	0	0	1	0	1
4	0	1	0	1	0	1	0	1	0
5	1	1	0	0	0	0	0	1	1
6	0	0	1	0	0	0	1	0	0
7	1	1	1	1	1	0	0	0	0
8	0	0	0	0	0	1	1	1	1

For a given value of Ma, the frequency of modulating signal resides at a constant, while the frequency of carrier signal varies between the frequencies of 125 Hz, 150 Hz, and 200 Hz to align with the load frequency of 50Hz. Increasing the carrier signal frequency raises harmonic levels; however, to mitigate switching losses, the carrier frequency is limited to 5 KHz.

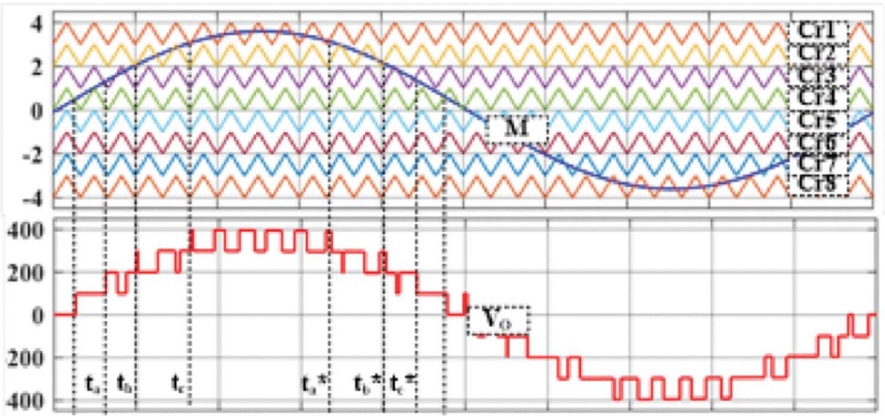


Figure 3. Schema of level-shifted PWM.

The estimation of capacitance values is imperative and that ensures the desired voltage of output under-appreciated ripple values. The output voltage levels are determined by the amount of capacitor energy, which includes charging and discharging. As illustrated in Fig. 3, the calculations procedure for capacitance values are considered by considering the maximum discharging intervals. The capacitor C1 is designed to deliver the ±2V dc and ±4V dc, while the capacitor C2 discharges at a value of ±3V dc and ±4V dc. As shown in Fig 3, the switching transitions, i.e., ta, tb, tc, ta*, tb*, and tc*for each voltage level are calculated by (1) - (6) [30]-[32].

$$t_a = \frac{\sin^{-1}\frac{1}{4}}{\omega_m} \quad (1)$$

$$t_b = \frac{\sin^{-1}\frac{2}{4}}{\omega_m} \quad (2)$$

$$t_c = \frac{\sin^{-1}\frac{3}{4}}{\omega_m} \quad (3)$$

$$t_a^* = \frac{\pi - \sin^{-1}\frac{1}{4}}{\omega_m} \quad (4)$$

$$t_b^* = \frac{\pi - \sin^{-1}\frac{2}{4}}{\omega_m} \quad (5)$$

$$t_c^* = \frac{\pi - \sin^{-1}\frac{3}{4}}{\omega_m} \quad (6)$$

Under resistive load circumstances, the highest discharging occurs at the ±4V dc voltage level. A substantial amount of voltage decline occurs within the time interval (tx − ty). When determining the capacitance values, careful consideration is given to extended discharging time intervals for each capacitor. It is noted that the charge or discharge cycles can occur multiple times within the (tx − ty) interval. The discharging time intervals for capacitor C1 are denoted as (tx1 − tx2), while the corresponding intervals for capacitor C2 are expressed as (ty1 − ty2).

4. RESULTS AND DISCUSSIONS

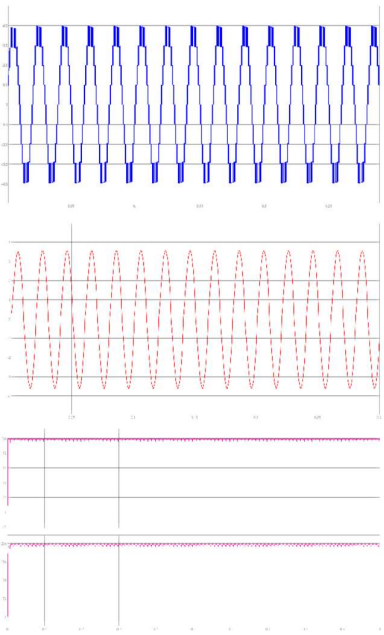
The merit of the present configuration can be substantiated through simulation outcomes, considering various component parameters under diverse load conditions. Specifically, the input fix at 100V DC, and the capacitor values are designated as C1 = 2200μF and C2 = 2200μF. The load at end side is as RL = 100ohm + 150mH with a Ma value of 1. Fig 4 indicates (from top to bottom) the MATLAB results of output responses such as voltages and currents. Figures 4 and 5 represent simulation results corresponding to output voltage, current and capacitor voltages under RL load and the switching frequency variations.

Table 2. Comparison of proposed work.

Parameters	References													
	2012 [14]	2013 [15]	2014 [16]	2014 [17]	2017 [18]	2018 [19]	2019 [20]	2021 [24]	2021 [25]	2022 [26]	2022 [27]	2022 [28]	2022 [29]	Proposed
Ns	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Nsw	13	12	8	10	10	17	18	12	14	9	12	10	11	8
N-drivers	13	12	8	10	10	17	18	11	14	9	12	10	11	8
ND	0	2	6	3	4	0	5	2	0	2	1	0	0	2
NC	3	2	3	3	3	4	4	4	5	5	2	2	2	2
G	4	4	4	4	4	1	4	3	4	4	4	4	3	4
MBV	4	4	4	4	4	4	4	3	4	2	4	4	3	4
TSV	6.25	6.25	8	6.25	7.5	7.25	7	7.5	7.5	10	7.5	6.25	5.53	6.25
N-total	16	16	17	16	18	21	27	18	19	16	14	12	13	12
No. of voltage levels	9	9	9	9	9	9	9	9	9	9	9	9	7	9
Efficiency (%)	85.9	83	91.5	91.6	93.5	NA	92.5	94.5	98.3	94	87 - 95.5	97	98.77	96.5

Table 2 provides a comprehensive comparison of various parameters across multiple references in the literature. The parameters include Ns (no. of stages), N-sw (no. of switches), N-drivers (no. of drivers), ND (no. of diodes), NC (no. of capacitors), G (Gain), MB (Minimum breakdown voltage), TSV (Total simulation time in milliseconds), N-Total (Total number of components), Number of Voltage Levels, and Efficiency (%). Each parameter is compared across different references spanning from 2012 to proposed solutions, with corresponding numerical values provided for each reference year. The table offers insights into the evolution and performance variations of different solutions over time, allowing researchers and practitioners to analyze trends and make informed decisions regarding the selection and optimization of circuit designs. Additionally, the efficiency percentages provide an indication of the overall effectiveness of the solutions, with higher values suggesting improved performance and energy utilization. This comparative analysis aids in identifying potential areas for further research and improvement in the design and implementation of electrical circuits.

The proposed configuration exhibits the capability to elevate the input voltage from 100V to 400V as voltage at output while maintaining equilibrium in capacitor voltages with C1 at 100V and C2 at 200V. The voltage THD of the output is recorded below 5%.



Time (Sec)

Figure 4. Output responses of (a) voltage, (b) current and (c) capacitor for RL load.

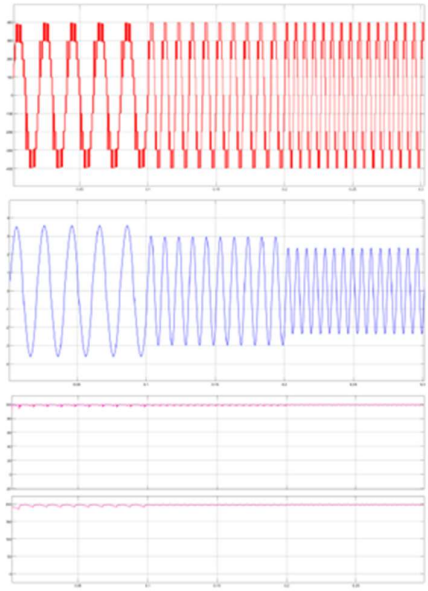


Figure 5. Output responses (top to bottom) of output voltage, current and capacitor voltage across capacitors.

5. CONCLUSION

This article introduces a brand-new nine-level inverter with a single DC supply that is intended for standalone solar PV installations. The suggested topology uses a parallel/series-charging/discharging method for capacitors and boasts quadruple voltage gain capabilities. The voltages of capacitors are balanced using LSPWM to produce the desired output voltage with the least amount of component stress. This topology's experimental setup can be adjusted to accommodate a range of situations, such as changing load scenarios, variation of input voltage,

switching frequency, changes in amplitude and frequency modulation and frequency adjustments. Both the output voltage's THD and the capacitors' voltage ripples fall well within permissible bounds of 5%. A comparative study shows that the suggested topology has a simple structure, fewer switches, the ability to boost quadruple, improved efficiency, affordability, and a lower Total Switching Stress (T.S.V). Results from MATLAB simulations support the effectiveness of the suggested design. Essentially, this novel topology provides a single DC source power solution for renewable solar PV applications that need triple voltage gain DC-AC power conversion and less switch- ing stress from fewer switches. The current work can be extended to emerging areas of RES and electric vehicles [35]-[37].

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